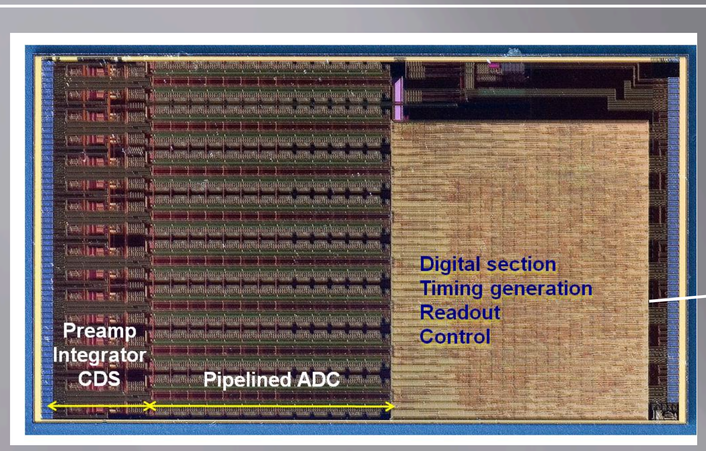
Integrated Circuits (IC) Capabilities

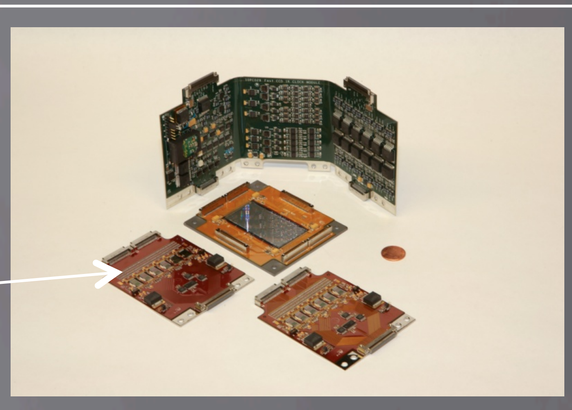
Lawrence Berkeley National Laboratory, Berkeley, CA (USA)

Field of expertise:

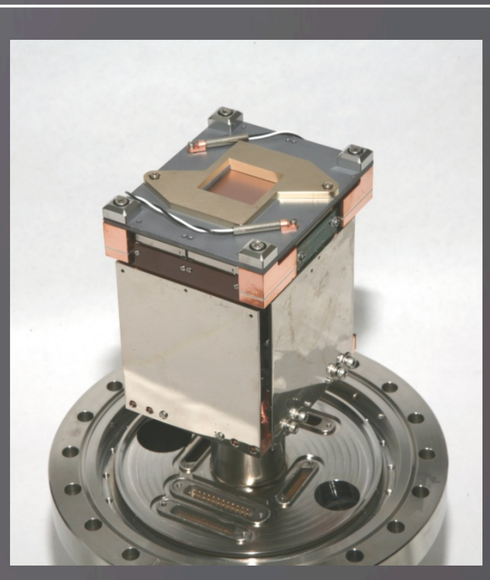
- Radiation hard circuit design for High Energy Physics experiments. (Up to 1 GigaRad total dose and Single Event Upset (SEU) tolerant).
- Mixed mode (Analog and Digital), System On a Chip (SOC).
- Low power, Low noise, High speed, High density circuitry.
- Specialized in deep submicron CMOS, Silicon On Insulator (SOI), High Voltage CMOS (120V), CMOS Opto, 3D technologies.



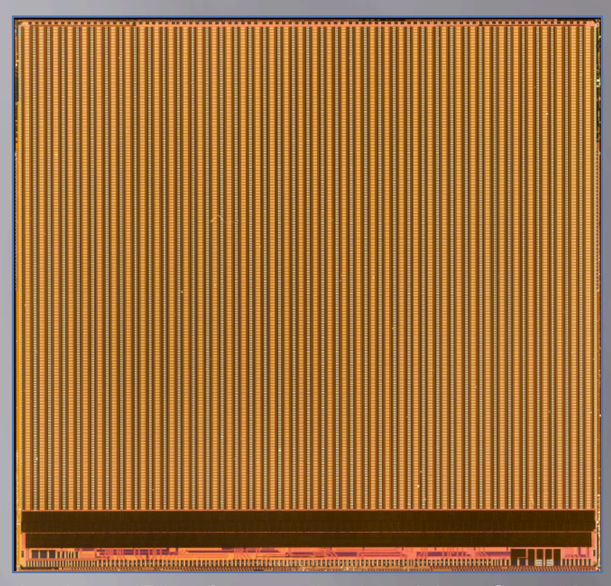
16 channels, 1MPixels/s, low noise, analog signal processor and digitizer for **Fast CCD Xray imaging**. Process 0.25μm CMOS.



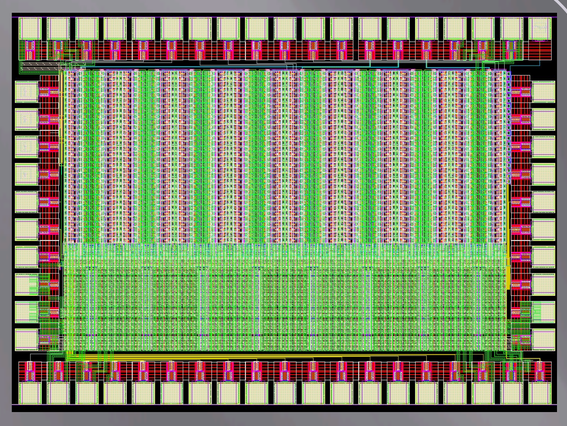
Circuit currently used in a compact 1K frame store fast CCD Xray camera at ALS and LCLS.



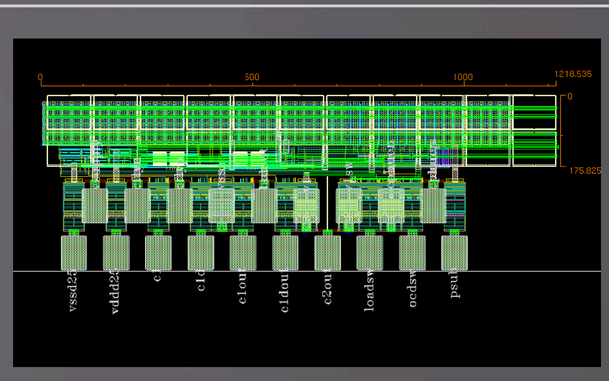
Fully assembled camera



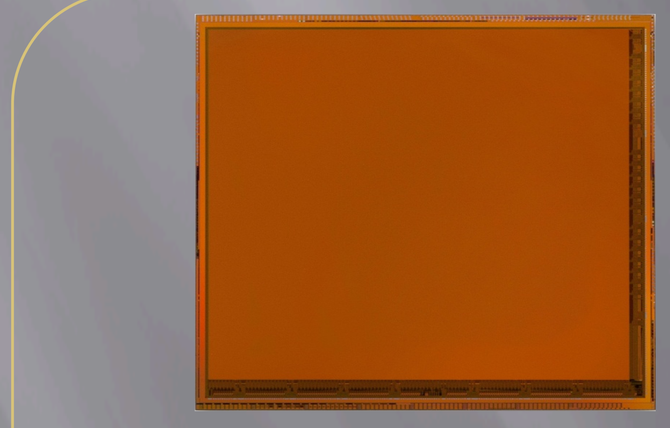
Active Pixel readout chip for the **ATLAS Pixel detector.** Reticle size**.** FEI4: 0.13μm CMOS. Pixel size: 50μmX250μm. ~ 20mm X 20mm



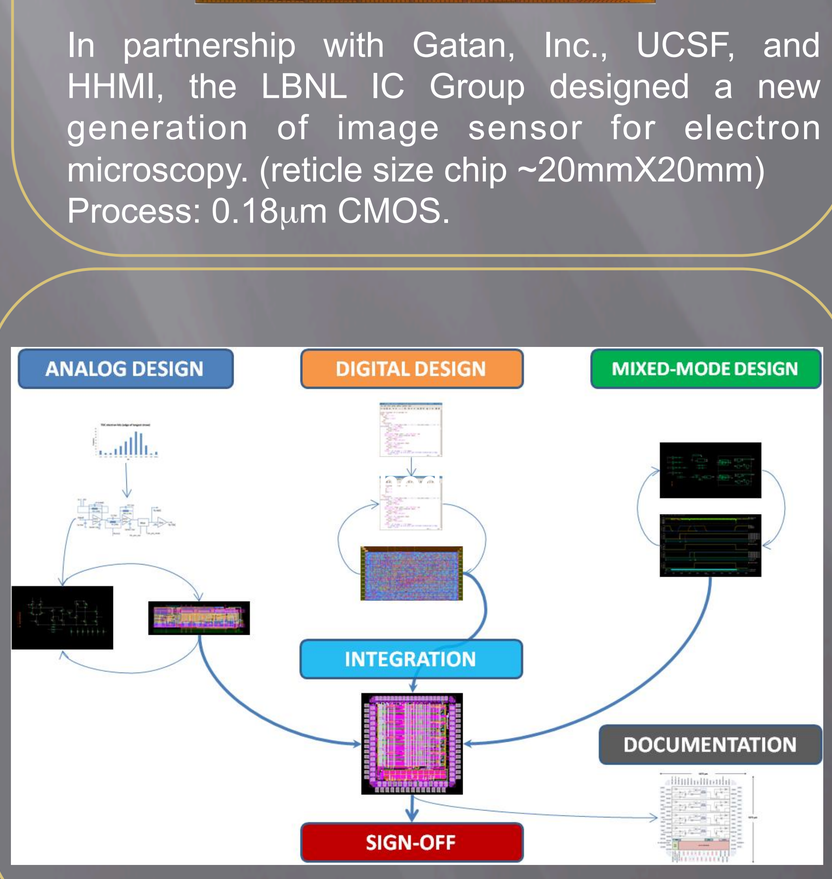
Evolution of the active pixel readout: Smaller pixel size: 25μmX125μm. Substantial area reduction. Room for more digital processing. Process: 65nm CMOS.

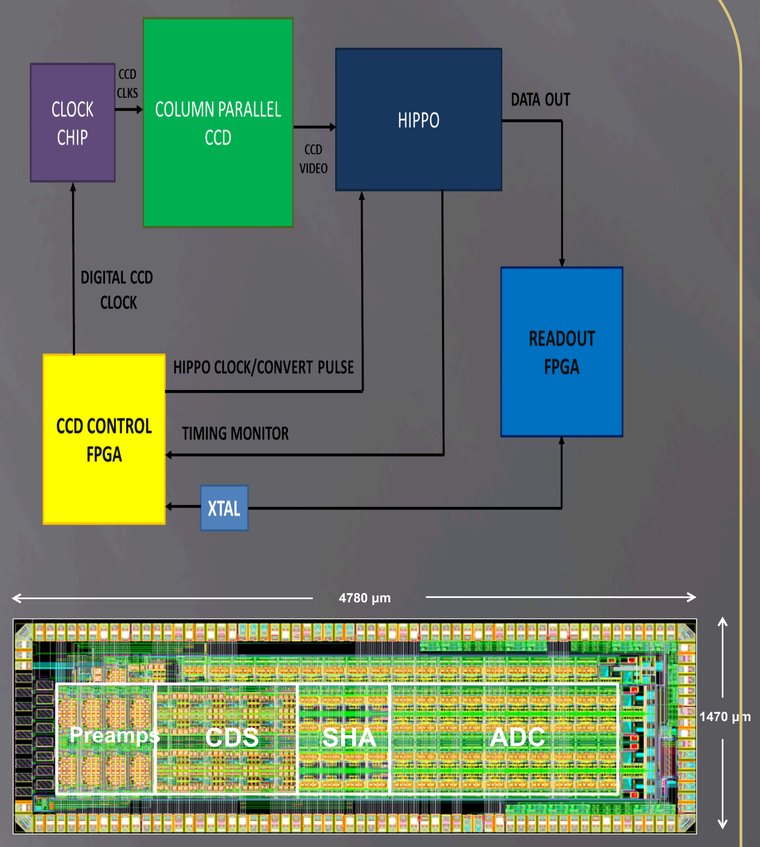


The LBNL IC group is developing high efficiency DCDC converters for many applications with LDRD funding: “High voltage up/down converter for low power, low density detector instrumentation”.
A 1.2V 4:1 down converter has been designed and submitted for fabrication as a test vehicle for low mass detectors in High Energy Physics
Process: 65 nm CMOS (in fabrication).

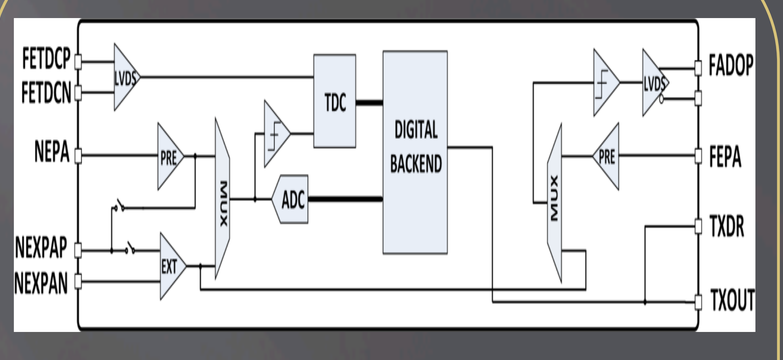


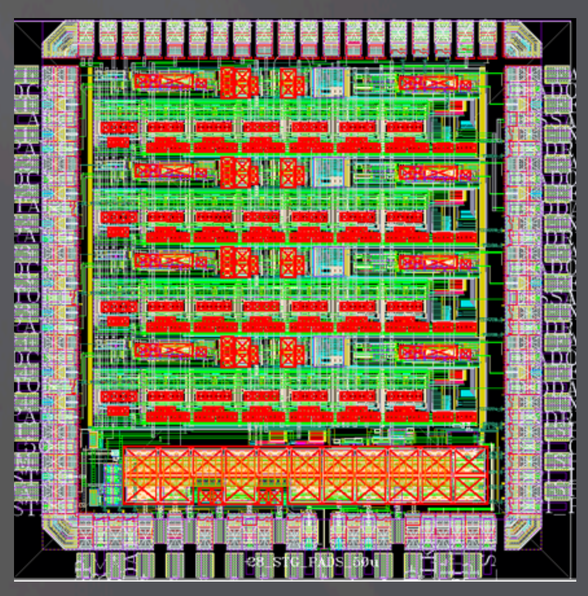
In partnership with Gatan, Inc., UCSF, and HHMI, the LBNL IC Group designed a new generation of image sensor for electron microscopy. (reticle size chip ~20mmX20mm)
Process: 0.18μm CMOS.





High-Speed Image Pre Processor with Oversampling (HIPPO) for very fast fully column parallel CCD readout.
10 Mpixels/s, 35e noise, 50μm pitch, 16 channels.
Process: 65nm CMOS.





Processor Of Muons decays (POM).
Low noise, Fast timing resolution (30ps) 65 MHz digitizer for wire chamber readout, (Mu2e experiment)
4 channels, 300μm pitch.
Process: 65nm CMOS (In fabrication).